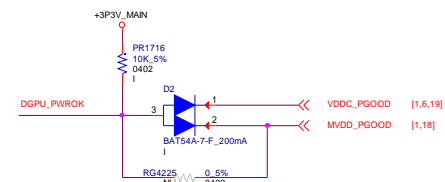
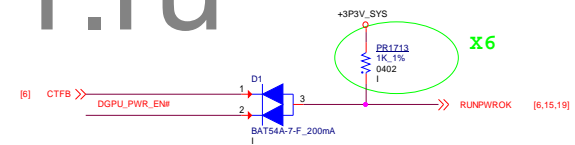
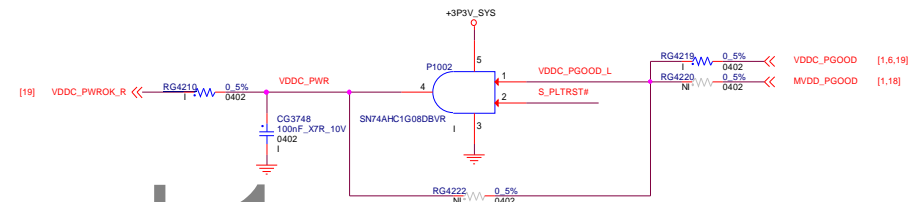
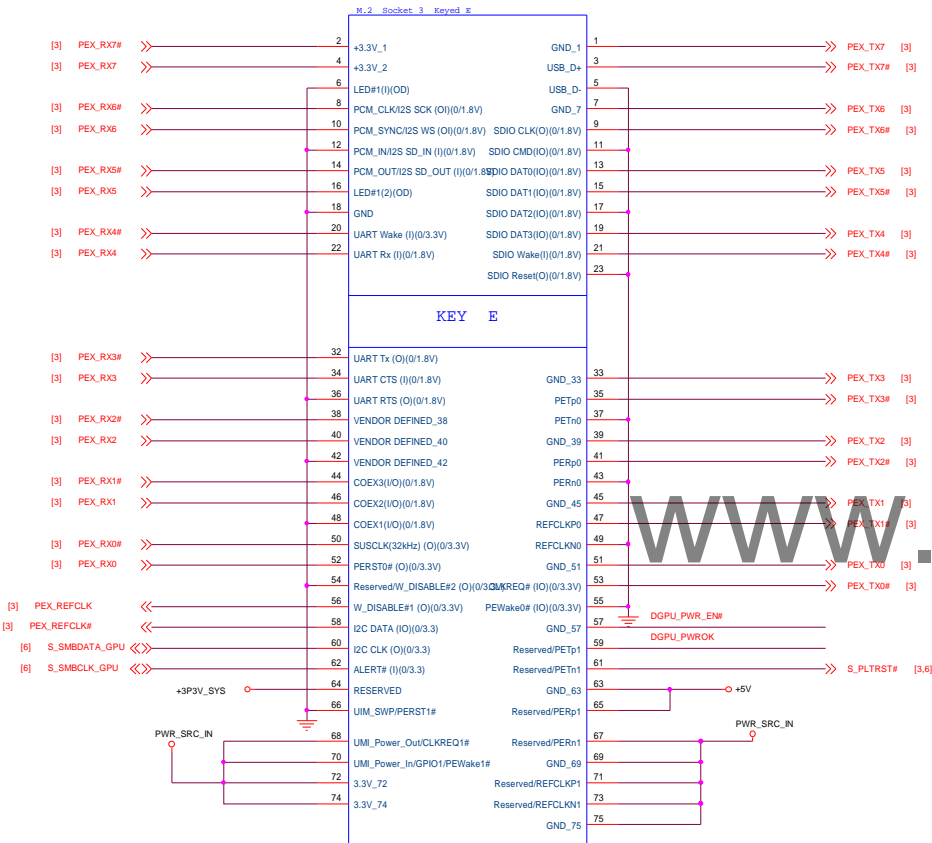
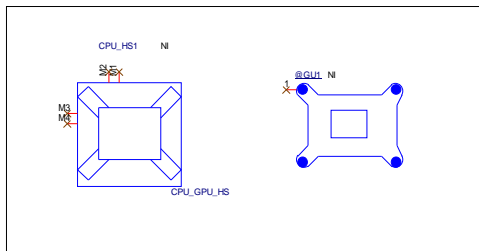


PWR:19.5V~3.92A; 5V~1.05A
3V~200mA



Footprint need update



PCB1

Printed Circuit Board

PCB_0101CFD04-575-H

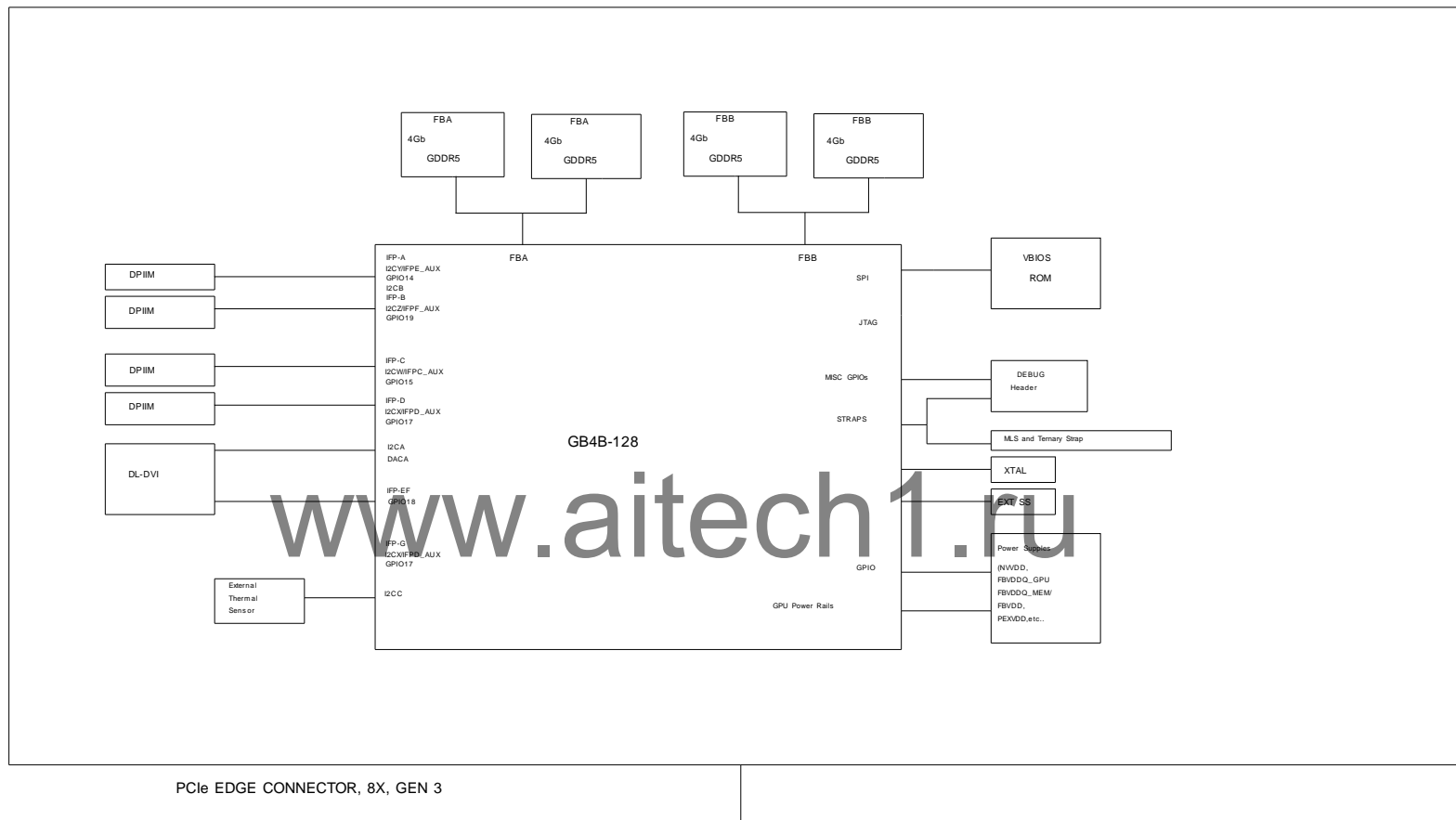
CCL=V

Description = 8-Layer PCB,Color With Green Soldermask,White Silkscreen,NPG-R,ML1,3.27X2.83inch,Rev:1.00,ROHS,HF

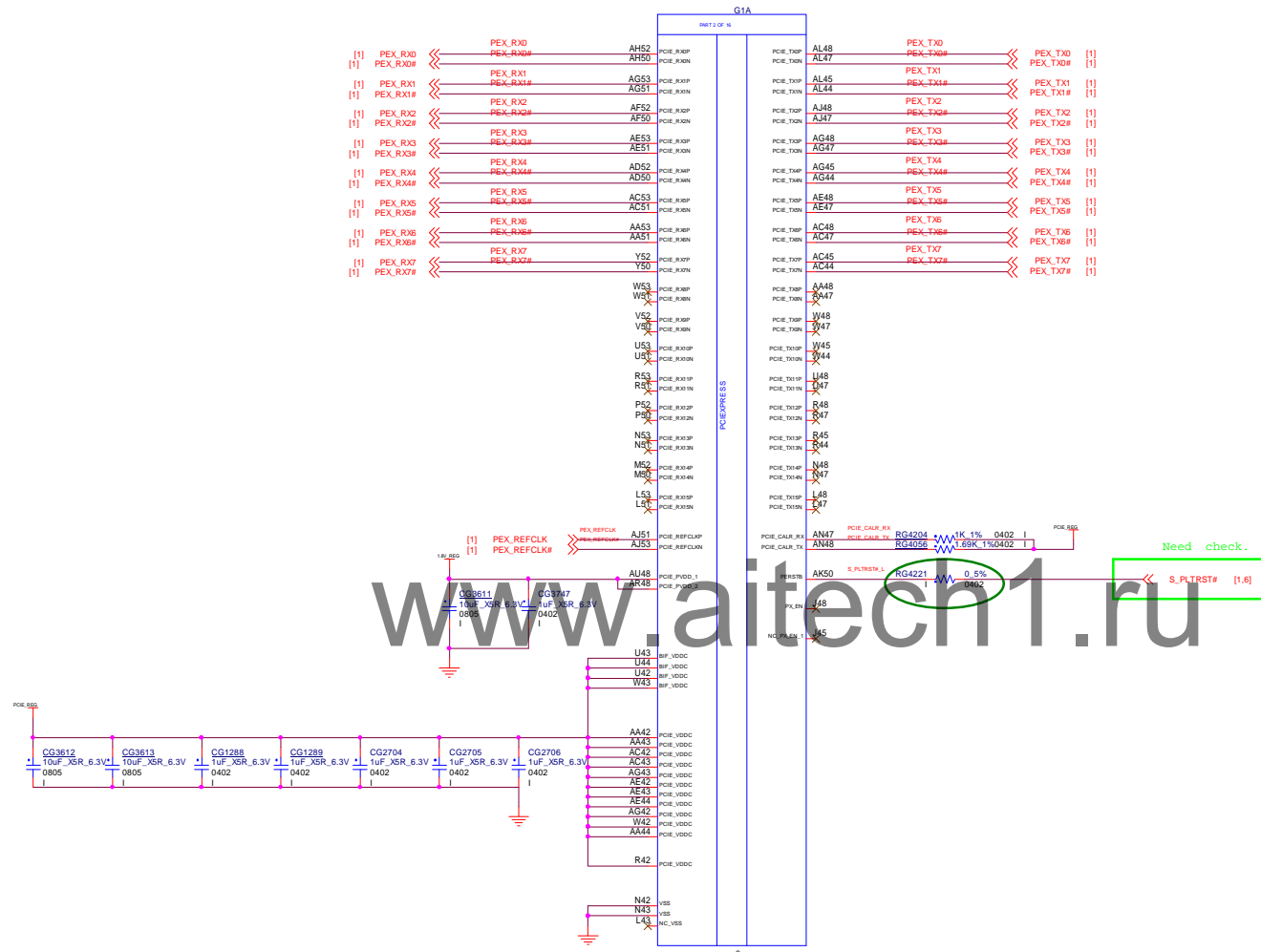
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M.2 Golden Finger	
Size	Document Number
Tesla	
Date: Monday, June 27, 2016	Sheet 1 of 21
Rev	X5

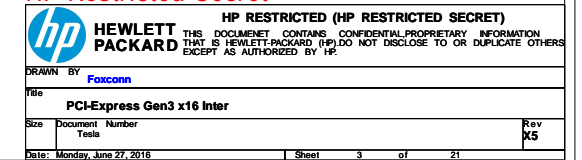
2. Block Diagram

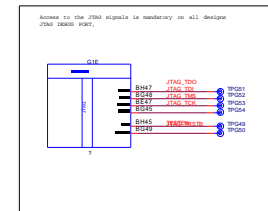
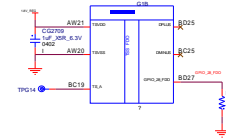
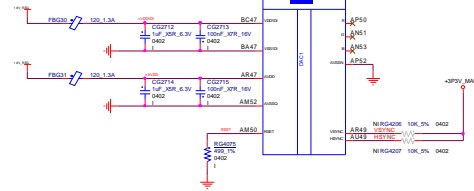


3. PCI-Express Gen3 x16 Interface

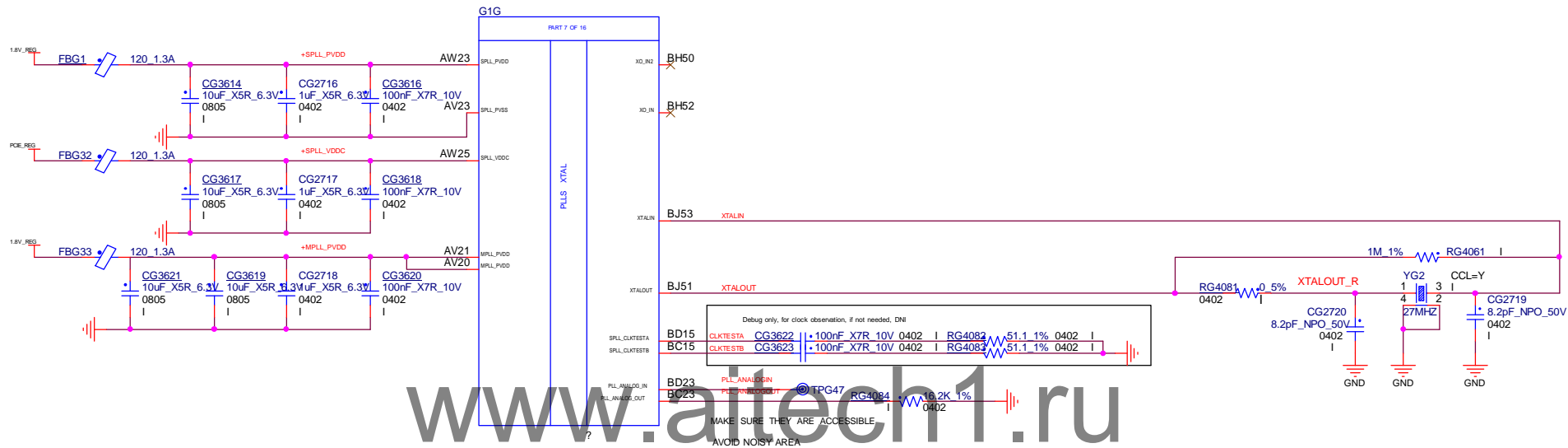


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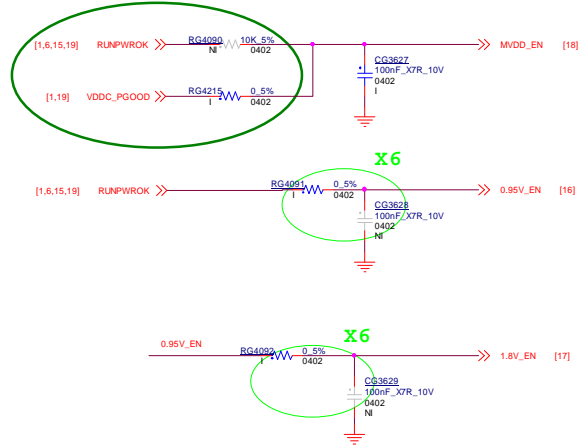
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Title Emerald CLK			
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	Tesla	X5	
Date: Monday, June 27, 2016		Sheet 5 of 21	

Power up Sequence Management

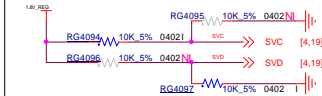
Example only. Parameters may need fine tuning. The following requirements from datasheet must be met:

- o All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/us.
- o It is recommended that the 3.3-V rail ramps up first.
- o The 3.3-V, 1.8-V, and 0.95-V rails must reach their ready states at least 10 us before VDDC and VDDCI start to ramp up.
- o The external pull ups on the DDCAUX signals (if applicable) should ramp up before or after both VDDC and VDD_CTH have ramped up.
- o The power rails that are shared with other components on the system should be gated for the dGPU so that when the dGPU is powered down (for example, AMD PowerXpress idle state), all the power rails are removed from the dGPU. The gate circuits must meet the slew rate requirement (such as <= 50 mV/us).
- o For power down, reversing the ramp-up sequence is recommended.



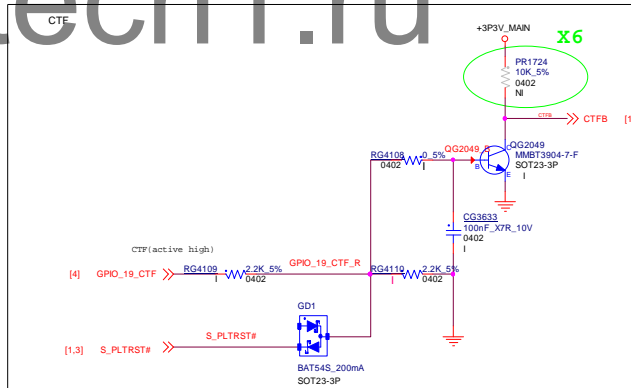
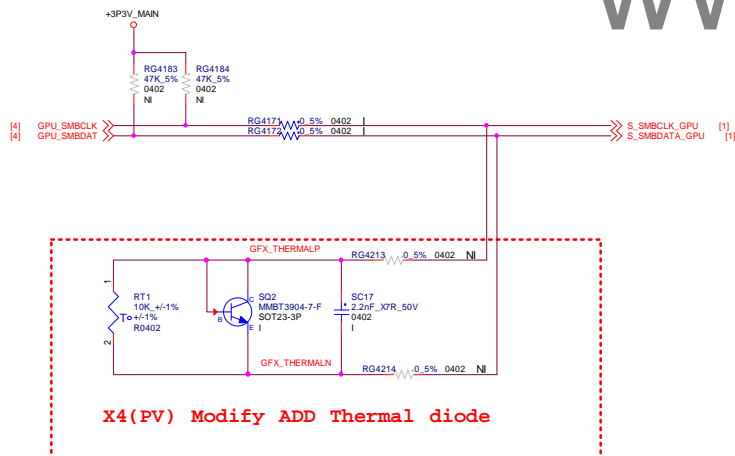
Pre-PWROK Output Voltage

SVC	SVD	V
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8



OPTIONAL EXTERNAL THERMAL SENSOR

+3PWROK should be shut off whenever dGPU is powered down (e.g., sleep states, Switchable Graphics iGPU mode, etc)




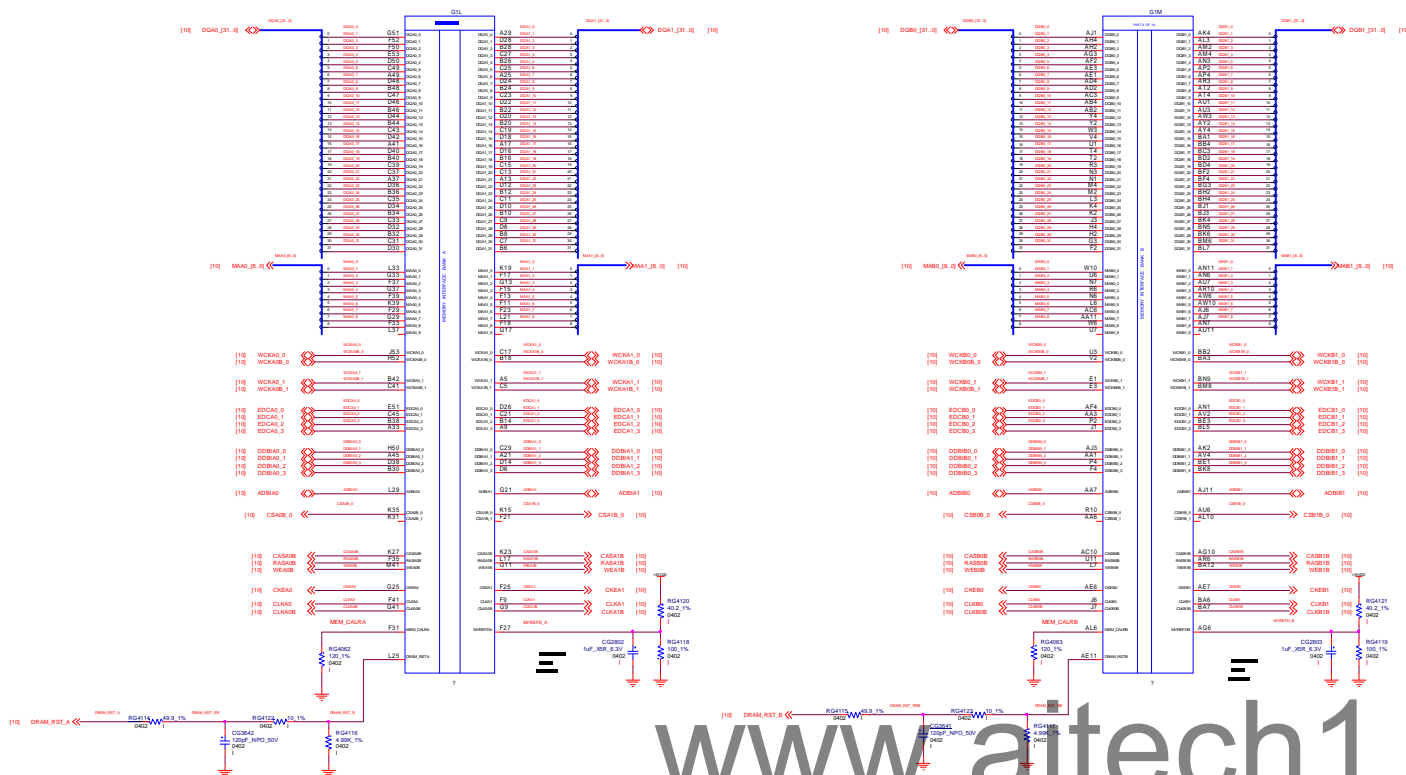
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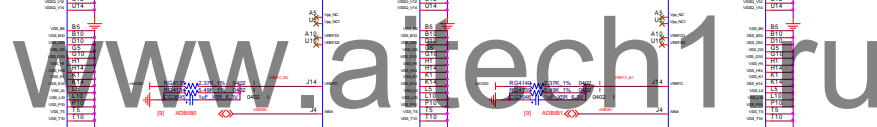
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	Tests	X5	
Date: Monday, June 27, 2016		Sheet	6 of 21

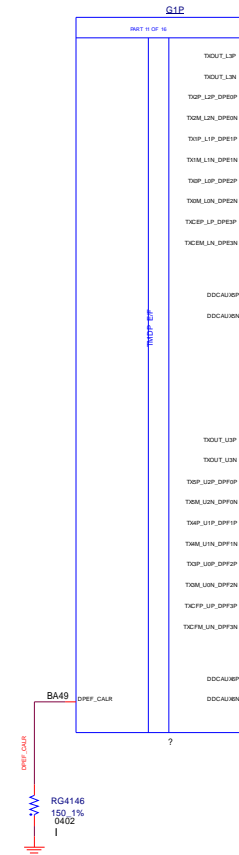



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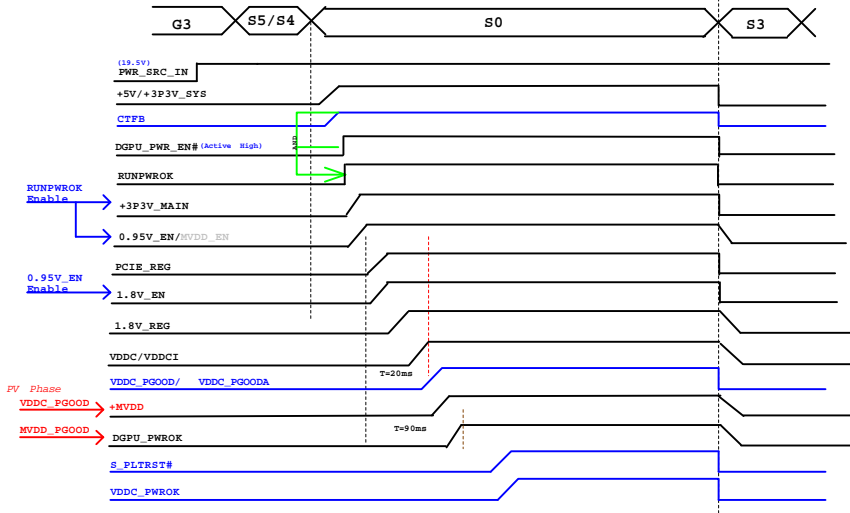




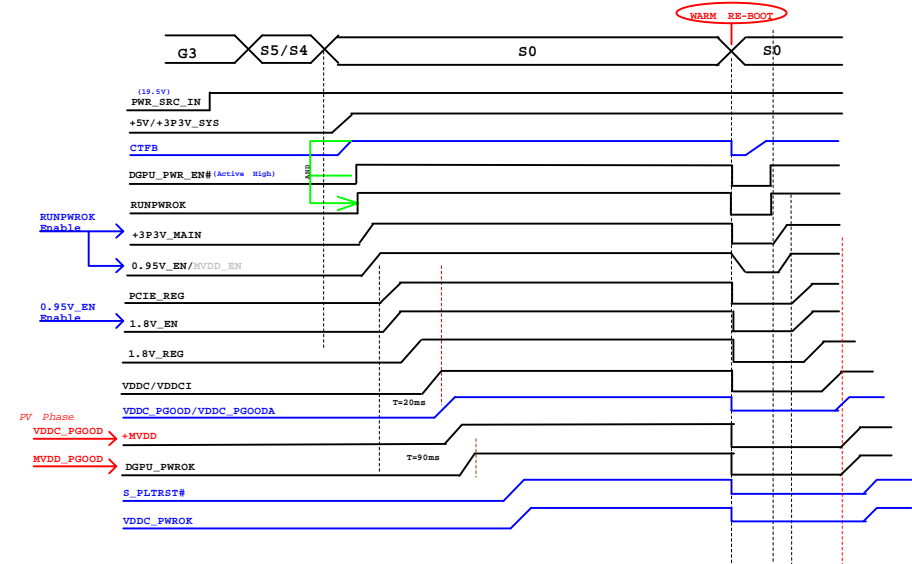


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File <u>Emerald TMDP_LVTMDP</u>			
Size	Document Number	Rev X5	
Date: Monday, June 27, 2016	Sheet	11	of 21

GPU POWER ON SEQUENCE DIAGRAM

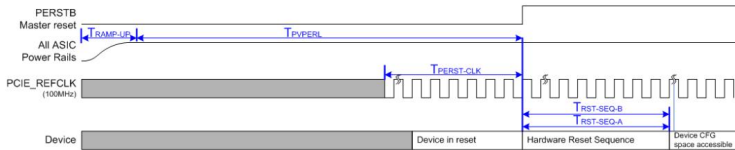


WARM RE-BOOT POWER SEQUENCE DIAGRAM

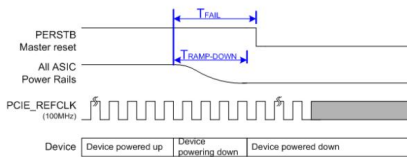


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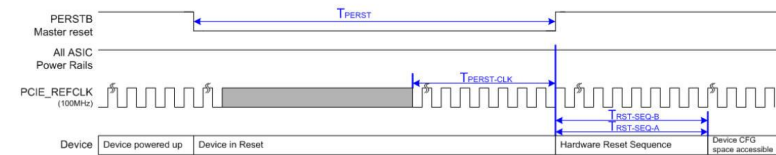
Cold-boot Sequence



Power Down Sequence



Warm-Boot Sequence




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DESIGNED BY: Foscom					
Title: Power Sequence					
Document Number: Test					
Date: Monday, June 27, 2023					
Sheet: 12 of 21					

X2 modify list:


Date	Action	reference	netname	Page	Description
2015.12.10	Modify			Page 4.	CG3741 change 680nF to 10nF and instaled
2015.12.11	Modify			Page 1.	Add RG4210 (0 ohm) and CG3748 (100nF) for filter noise.
2015.12.15	Modify	GPIO_5		Page 4.	G1D pin BH35 change netname to GPIO_5
		VSYNC, HSYNC			G1F pin AR49 change netname to VSYNC and pinAU49 change netname to HSYNC.
		WP#			UG2013 pin 3 change netname to WP#.
		VDDR4, GENLK_VSYNC			G1C pin AV38, AV39, AW38, AW39 chagne netname to VDDR4 and pin BD35 change netname to GENLK_VSYNC.
		QG2049_B		Page 6.	QG2049 pin B change netname to QG2049_B
		GPIO_19_CTF_R			After GPIO_19_CTF through RG4109 change netname to GPIO_19_CTF_R
		MVREFD_A		Page 9.	G1L pin F27 change netname to MVREFD_A
		MEM_CALRA			UNNAMED_30_BONAIRE_I313_MEMCALRA change to MEM_CALRA
		MEM_CALRB			UNNAMED_30_BONAIRE_I314_MEMCALRB change to MEM_CALRB
		ZQ_B0		Page 10.	M2 pin ZQ change netname to ZQ_B0
		ZQ_C0			M3 pin ZQ change netname to ZQ_C0
		ZQ_D0			M4 pin ZQ change netname to ZQ_D0
2015.12.24	Modify			Page 4.	UG2013 change SST25VF512A-33-4C-SAE (512Kb) to MX25L1006EMI-10G (1Mb) RG4197 change 4.53k ohm to 3.24k ohm RG4198 change 2k ohm to 5.26k ohm
2016.04.19	Modify			Page 3.	Add RG4221 0ohm to prevent debug.
				Page 6.	Add thermal sensor circuit, SQ2, RT1, SC17, RG4213 and RG4214.
					Add RG4215 0ohm connect to VDDC_PGOOD for MVDD timing changed following CRB sch.
				Page 19.	Add RG4218 0ohm short VDDC_PGOOD and VDDC_PGOODA following CRB sch.
					Add RG4224 0ohm for debug
				Page 1.	Add RG4223 0ohm and RG4216 0ohm to DGPU_PWROK, using PGOOD control the sequence.
		S_PLTRST#			Using D2 do a AND gate S_PLTRST# and VDDC_PGOOD, that control the VDDC_PWROK of FU1000 resend again after S_PLTRST#.
		VDDC_PGOOD			Delet D3 and GD2 for change design,
		S_PLTRST#			add P1002 AND gate to control the VDDC_PWROK of FU1000 resend again after S_PLTRST#.
					And add RG4219 0ohm and RG4220 0ohm for prevent wrong sequence control.

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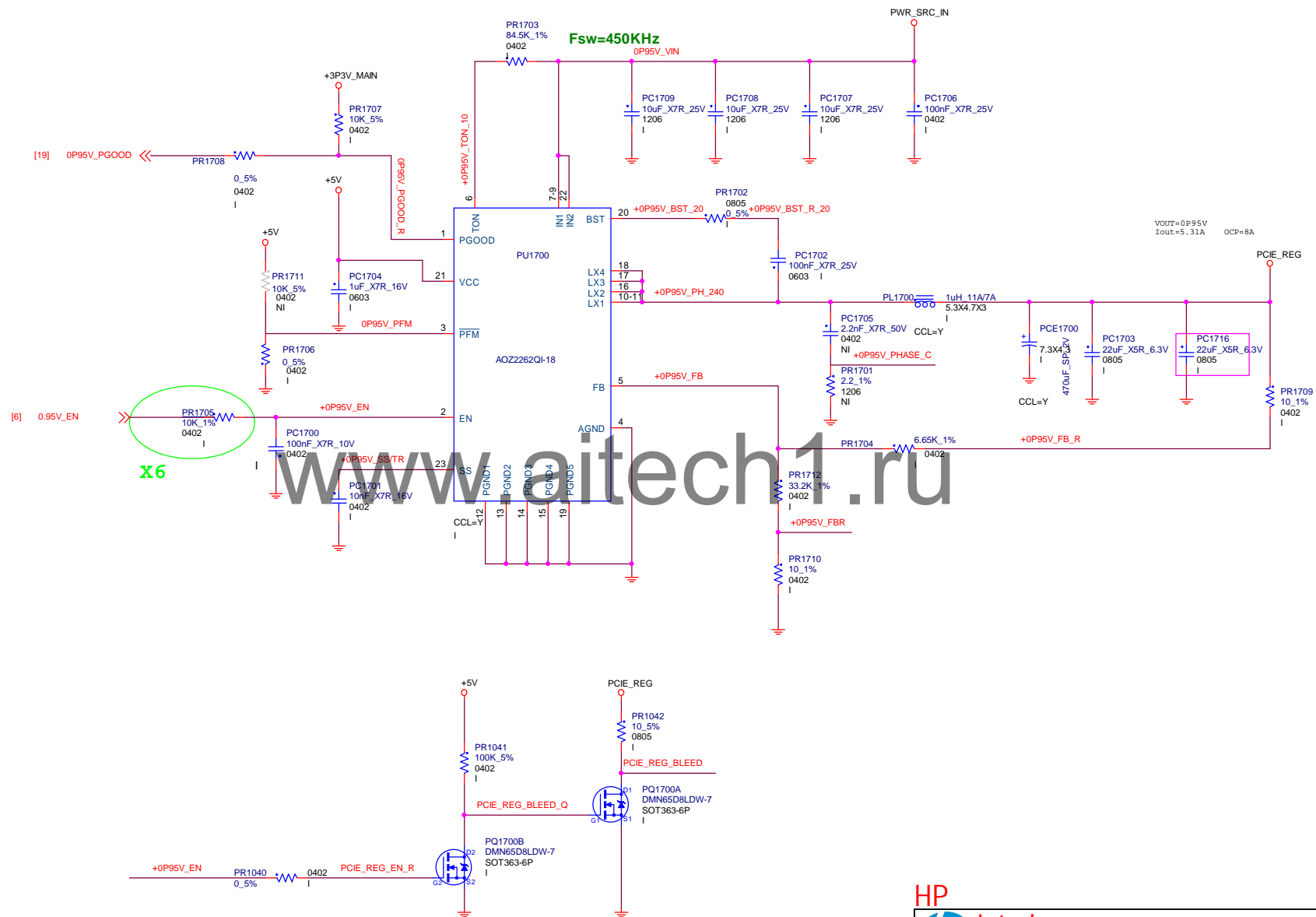
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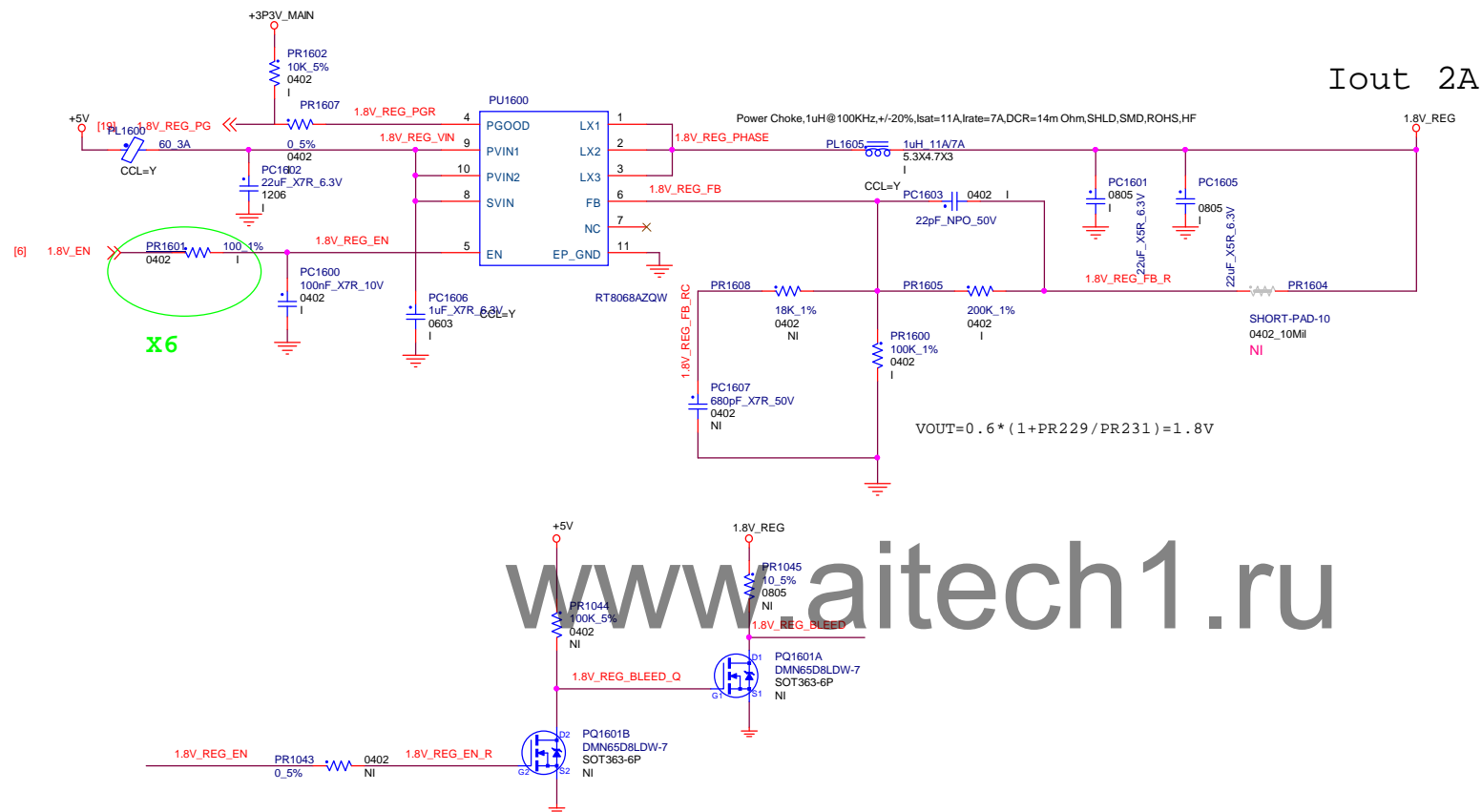
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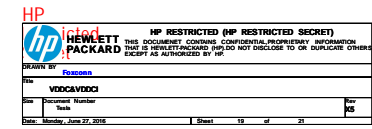




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[illegible]

X2 modify list:

Date	Action	reference	netname	Page	Description
201512.2	Modify			P16	PCIE_REG: Add PC1716(22uF) for phase margin fail.
				P17	
				P18	1.8V_REG: delete PC1604 for timing fail.
					MVDD: change PR1513 to 1k, change PC1503 to 2.2nF for phase margin fail. Add bleed off circuit for timing fail.
201512.7	Modify			P18	POWER SEQUENCE: Change PQ1557 and PQ1558 to Dual MOSFET PQ1557A and PQ1557B
201512.8	Modify			P19	Add ehotpad (RJP1212,RJP1213,RJP1222,RJP1223,RJ1232,RJP1233,RJP1252,RJP1253)
201512.26	Modify			P16	Change PD1700 to A0Z2262Qi-18 for efficiency fail issue.
20160414	Modify			P16	Add discharge circuit for PCIE_REG fall time issue.(PR1040,PR1041,PR1042,PQ1700)
				P17	Add discharge circuit for 1.8V_REG fall time issue.(PR1043,PR1044,PR1045,PQ1601)
				P18	PR1506 value from 10K to 10.5K.
20160426	Modify			P1	Add PR1716, D2 and RG4225 for correct DGPU_PWR0K signal. Remove D3 and GD2, change D2 to P1002 AND gate for correct VDDC_PWR0K.
				P6	Add VDDC_PGOOD and RG4215 for MVDD change power sequence.
					Add SQ2, RTL, SC17, RG4213 and RG4213 for thermal diode.
					Change PR1713 from 10k ohm to 1k ohm for power sequence.
20160627	Modify			P1	Change PR1713 from 10k ohm to 1k ohm for power sequence.
				P6	Change RG4091 and RG4092 from 10k ohm to 0 ohm for power sequence. CG3628, CG3629 and PR1724 remove for power sequence.
				P16	Change PR1705 from 0 ohm to 10k ohm for power sequence.
				P17	Change PR1601 from 0 ohm to 100 ohm for power sequence.

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